IN THE CLAIMS:

1. (Currently Amended) A continuous time sigma delta converter comprising:
conversion means ~~(510, 520, 530, 540, 560)~~ having known non-ideal characteristics and arranged to provide an output signal;
a compensation circuit ~~(570)~~ comprising error modelling components ~~(370, 375, 380, 385, 390, 395)~~ arranged to substantially model the non-ideal characteristics of the conversion means ~~(510, 520, 530, 540, 560)~~; and
summation means ~~(490)~~ coupled to combine the compensation signal with the output signal in order to provide a compensated output signal.

2. (Currently Amended) The converter of claim 1 further characterised by[[:]] the summation means ~~(580)~~ being arranged to subtract the compensation signal from the output signal in order to provide the compensated output signal.

3. (Currently Amended) A compensation circuit ~~(570)~~ for use with a continuous time sigma delta converter ~~(510, 530, 540, 560)~~ having known non-ideal characteristics, the compensation circuit ~~(570)~~ comprising error modelling components ~~(370, 375, 380, 385, 390, 395)~~ arranged to substantially model the non-ideal characteristics of the converter ~~(510, 530, 540, 560)~~ in order to provide a compensation signal,
wherein the compensation signal is combinable ~~(580)~~ with a non-ideal output of the converter ~~(510, 530, 540, 560)~~ in order to provide a compensated output signal.

4. (Currently Amended) A method for compensating for known non-ideal characteristics in a continuous time sigma delta converter ~~(510, 530, 540, 560)~~, the method comprising:
converting an input signal of one time domain to an output signal of another time domain using a converter ~~(510, 530, 540, 560)~~ having known non-ideal characteristics;
modelling the non-ideal characteristics of the converter in a compensation circuit ~~(570)~~;
combining a compensation signal output of the compensation circuit ~~(570)~~ with the output signal of the converter ~~(510, 530, 540, 560)~~ in order to provide a compensated output signal.

5. (Currently Amended) The converter of claim 1 ~~or claim 2, circuit of claim 3 or method of claim [[4]]~~ further characterised by[[:]] the non-ideal characteristics being associated with a feedback path ~~(540)~~ of the converter.

6. (Currently Amended) The converter~~, circuit or method of any preceding claim~~ of claim 1 further characterised by[[:]] the non-ideal characteristics including symmetrical errors ~~(235)~~ associated with non-ideal rising and falling edges ~~(230)~~ of signal transitions of the converter ~~(510, 530, 540, 560)~~.

7. (Currently Amended) The converter~~, circuit or method of any preceding claim~~ of claim 1 further characterised by[[:]] the non-ideal characteristics including asymmetrical ~~(245)~~ errors associated with non-ideal rising and falling edges ~~(230)~~ of signal transitions of the converter ~~(510, 530, 540, 560)~~.

8. (Currently Amended) The converter~~, circuit or method of any preceding claim~~ of claim 1 further characterised by[[:]] the compensation circuit ~~(570)~~ having calibration parameters ~~(375, 395)~~ determined by an dichotomy technique which iteratively refines the values of the calibration parameters ~~(375, 395)~~.

9. (Currently Amended) A method for producing calibration parameters for use in the compensation circuit ~~(570)~~ of claim 1 ~~any preceding claim~~, the method comprising the steps of:
collecting output samples from the converter ~~(510, 530, 540, 560)~~;
calculating a Signal to Noise and Distortion Ratio of the collected data;
determining whether the calculated Signal to Noise and Distortion Ratio meets specified performance criteria;
selectively recalculating the Signal to Noise and Distortion Ratio in dependence upon the step of determining, using a calibration algorithm ~~(600-695)~~.

10. (Currently Amended) The method of claim 9 wherein the calibration algorithm uses a dichotomy technique ~~(600-695)~~ which iteratively refines the values of the calibration parameters.

11. (New) The circuit of claim 3 further characterised by the non-ideal characteristics being associated with a feedback path of the converter.

12. (New) The method of claim 4 further characterised by the non-ideal characteristics being associated with a feedback path of the converter.

13. (New) The circuit of claim 3 further characterised by the non-ideal characteristics including symmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

14. (New) The method of claim 4 further characterised by the non-ideal characteristics including symmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

15. (New) The circuit of claim 3 further characterised by the non-ideal characteristics including asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

16. (New) The method of claim 4 further characterised by the non-ideal characteristics including asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

17. (New) The circuit of claim 3 further characterised by the compensation circuit having calibration parameters determined by an dichotomy technique which iteratively refines the values of the calibration parameters.

18. (New) The method of claim 4 further characterised by the compensation circuit having calibration parameters determined by an dichotomy technique which iteratively refines the values of the calibration parameters.